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Development of HW/SW Platform for Real-Time Tests of Radar Front-End Module for Radar Machine Learning

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Abstract. In this paper, we developed a hardware and software platform of a real-time data logging system to verify radar front-end module (FEM) and signal-processing algorithms. We developed the hardware platform based on a field-programmable gate array (FPGA) and digital signal processor (DSP) and implemented firmware software to verify the various FEMs. Moreover, we designed a PC-based software platform to control radar logging parameters and acquired radar data. The developed platform was verified using a 24-GHz multiple-channel frequency-modulated continuous wave (FMCW) FEM in an environment of stationary and moving targets in a test chamber. Moreover, we verified human classification based on machine learning algorithm using the real measurement data.

Keywords; Radar system, data logging system, radar, FPGA, DSP

1. Introduction

Recently, radar systems have been applied for various applications, such as defense, aviation, automotive, medical, and security. In particular, since chip-set vendors have released various radar transceiver chips, and powerful digital signal processors (DSPs) and micro controller units (MCUs) on the market, it is expected that radar systems will have more commercial applications.

Radar systems consist of a front-end module (FEM) and back-end module (BEM) [1–3]. Here, the FEM is also divided into an antenna and a transceiver. The BEM comprises the hardware, including micro-processor and peripheral devices as well as embedded software, including signal-processing algorithms and operating functions. In

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each radar system, the configurations of FEM and BEM are based on the application area. For example, the field of view (FOV), types of antennas, wave-modulation method, transmitter power, controller type for signal processing, interfaces, and complexity of algorithms all vary.

Thus, in development of a radar system, the errors and performance of various FEMs and software including algorithms should be corrected and verified based on the signals obtained in the real field. Therefore, in the development of a radar system, a customized verification test-bed is typically also developed. However, it additionally requires time and cost.

Thus, in this study, we developed a hardware and software platform for real-time tests of various radar FEMs and signal-processing algorithms. The platform developed in this paper is comprising of hardware platform with a field-programmable gate array (FPGA) and digital signal processor (DSP) and software platform to control in/out pins and store data. The developed platform was verified using a 24-GHz multiple-channel frequency-modulated continuous wave (FMCW) FEM in a test chamber. Moreover, we verified human classification based on machine learning algorithm using the real measurement data.

2. Development and Implementation

A. HW and SW Platform Architecture

Figure 1 presents a block diagram of the system architecture of the hardware and software platform for real-time data logging. The platform comprises a logging module, a camera module, a PC with a graphic user interface (GUI), and an Ethernet-hub. The logging module comprises an analog digital converter (ADC), FPGA, and DSP to digitalize the received radar signal from the FEM, store these data, and control system management. In two network cameras, video files are stored together with radar logging data in real-time to verify the radar signal-processing results. The software block in the PC receives the logged radar data and verifies algorithms. Here, through the GUI, the user can control the whole platform. The logging module, camera module, and PC are connected through the Giga-bit Ethernet.

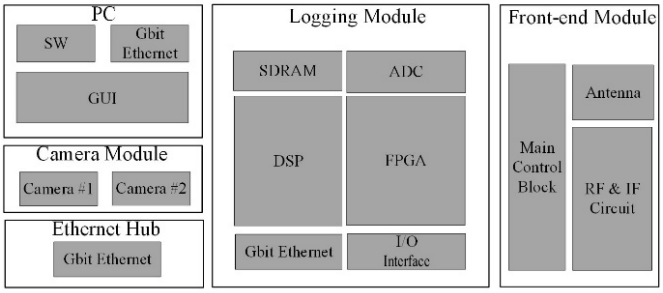


Fig 1. Block diagram of system architecture of hardware and software platform for real-time data logging.

B. HW Platform Architecture

Figure 2 shows the hardware block configured with an FPGA and a DSP. In this paper, we employ Intel's Stratix4 EPSE530H chip implemented to support an 8-channel ADC at the same time and TI TMS320C6450 operated with a 1-GHz clock. To store large amounts of data in real time, we employ two 256-Mbyte DDR2 SDRAMs.

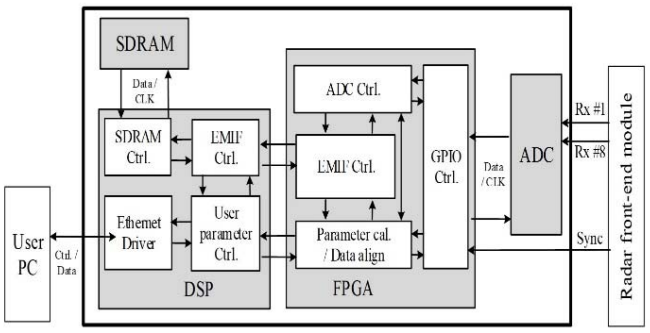


Fig 2. Block diagram of the designed data-logging board.

The received signals of the FEM are fed into the FPGA through the ADC, and control signals such as 'Sync' and 'RF_on' are connected through general purpose input-output (GPIO) pins of the FPGA. The DSP controls the SDRAM to store or read logged data and transfer these data to the PC through the Ethernet.

Between the FPGA and the DSP, the logged radar data are transferred to the external memory interface (EMIF) at high speed, and control signals are connected using GPIO pins. Moreover, the DSP and FPGA control the ADC, align digitalized samples, and store these data, which is based on user parameters selected on the GUI. For these tasks, the FPGA and DSP are designed with various internal blocks as shown in Figure 2.

Figure 3 shows a real photo of the hardware platform. In the layout of the printed circuit board (PCB), the placement and routing of chips and lines are optimized. As separating analog signals and digital clock lines as much as possible, we designed the platform so that digital noise will not affect the analog signals.

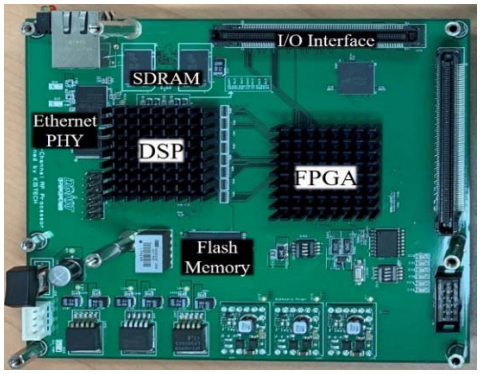


Fig 3. Photo of data-logging board implemented with main chips.

C. SW Platform Architecture

Figures 4 shows a block diagram of the software platform associated with the hardware platform. The developed GUI to manage radar data logging is also shown in Figure 5. The software platform comprises FPGA firmware SW, DSP firmware SW, and PC SW with a GUI.

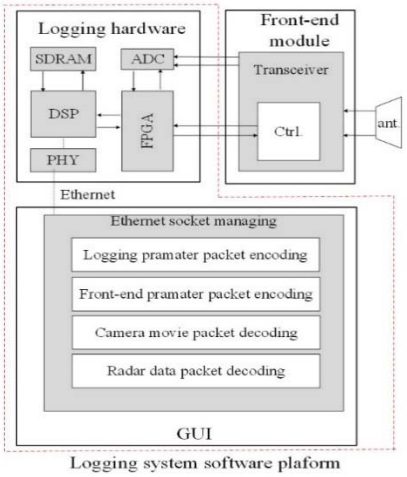


Fig 4. Logging system SW platform block diagram.

First, the PC software is operated with the GUI in the following steps.

- As setting Ethernet IP address on the GUI, the Giga-bit network is connected with the DSP through the PC SW.
- The user can select the logging mode and parameters, such as active channels, trigger mode, sampling frequency, number of ramps, and number of frames. This information is transferred to the DSP through the PC SW, and all logging conditions are ready at that time.
- The user can select 'START' and 'STOP' buttons on the GUI, and then the PC SW commands that the DSP SW should control starting and termination of data logging. At the same time, the PC SW can read video files and record log information.
- If the PC SW receives the logging completion message from the DSP SW, the PC SW stores radar data and video files in storage devices. These statuses are displayed as log messages on the GUI.

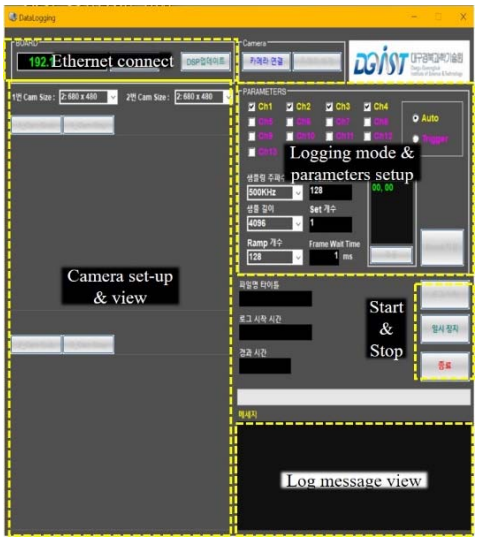


Fig 5. GUI to set user defined parameters.

Second, the FPGA firmware SW is operated as follows.

- Based on parameters transferred from the DSP, the ADC registers are set.
- If the start command is received from the user interface, the FPGA activates the 'RF_On' signal to wake the FEM and receives the digitized radar signals. Here, these data can be stored in synchronization with the 'Sync' signal or may be asynchronously stored. The user can select two modes using the GUI.

- When the data logging is completed, the FPGA informs the DSP SW about such completion.

Finally, the detailed procedures of the DSP firmware SW are summarized as follows.

- Based on parameters determined by user, the values are modified according to the DSP environment.
- If the save completion of the FPGA SW is monitored, the DSP requests ADC data and then stores all of the data into SDRAM memories.
- When the save is completed, the DSP sends the logging stop command to the FPGA SW and then transfer the stored data to the PC.

All schematics and codes for the FPGA firmware software are designed and synthesized based on the *Quartus II* tool. Moreover, we code and compile the DSP firmware software based on *Code Composer* tool

3. Verifications and Measurements

To verify the developed HW and SW platform, we carried out tests in a test chamber. The detail specifications and configurations are described in Table I and Figure 6 [4-5].

TABLE I. CHAMBER SPECIFICATION

Parameters	Specifications
Chamber Style	Rectangular
Chamber Size	10 m(L) × 5 m(W) × 4 m(H)
Shielding Frequency Range	8 GHz ~ 110 GHz
Shielding Effectiveness	60 dB at 8 GHz
Absorver Type	Microwave Absorber
Absorber Thickness	More than 8 inch
Absorber	More than -40 dB at 8 GHz

Moreover, we employed an FEM with eight receive channels developed in Korea RRC (Radio Research Center) team. The center frequency was 24 GHz, the bandwidth was 2 GHz. The vertical and horizontal FOVs of patch-type Tx and Rx antennas were 90. For antennas were mounted at half wavelength intervals. In this study, we designed a frequency-modulated waveform with a 250-MHz bandwidth, modulation period of 100

us, and ramp repetition period 1ms. In this study, we considered 3 scenarios. In the first scenario, a moving target placed at 2.1 m to 4 m was considered in chamber. Next, we tested the target detection algorithm in case of two walking human under indoor environment, Last, we also verified the moving human classification algorithm in the hall way of building. We set the sampling rate at 5 MHz, sample length as 500, the number of ramps as 128, and the number of frames as 1024 for the data-logging parameters. All received radar data was analyzed using algorithms coded by the *Matlab* tool.

Fig 6. Photo of chamber to verify the logging system with radar front-end module.

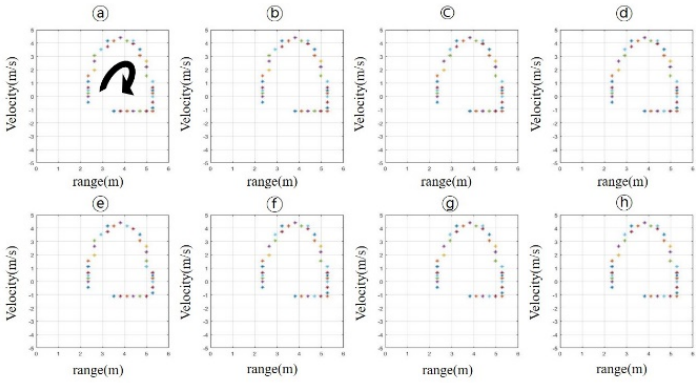


Fig 7. Range-profile results of the moving target in each channel: (a) to (h) indicates result of each Rx channel.

First, Figure 7 shows the results of overlapping detections of a moving target over several frames. Figures (a) to (h) present the range-velocity of each detection on channels #1 to #8. Here, the x-axis (meter) is range, and the y-axis is velocity (m/s). As

seen in the figure the target accelerated from about 2.1 m to 4 m, then decelerated, stopped at 5.2 m, and then returned to the origin position with a constant speed. Through these results, we can confirm that detections were consistent with the path of the true moving target in the chamber room.

Second, Figure 8 shows the detection results of two moving human in the several frames. The x-axis and y-axis indicate angle (degree) and range (meter).

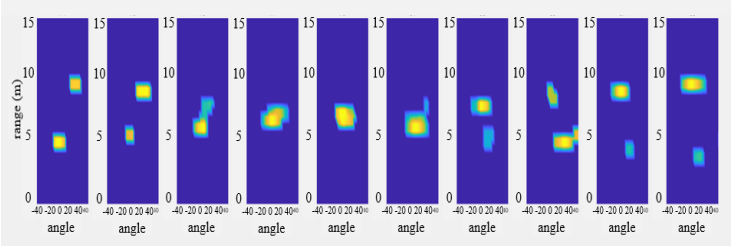
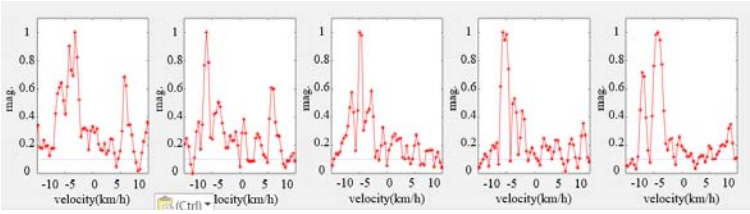


Fig 8. Detected range and angle of two moving human of the sucessive 10 frames.

(a)



(b)

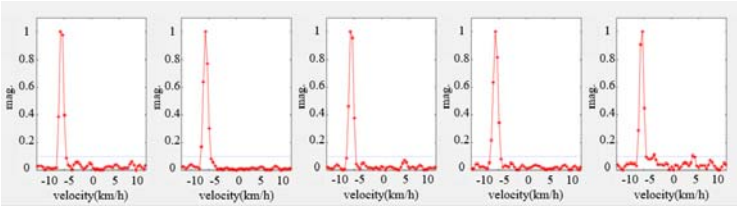


Fig 9. Doppler spectra of detection of walking human and moving vehicle over the successive five frames.

Finally, Figure 9 shows the Doppler spectra of detections in the several frames. The x-axis and y-axis indicate velocity (km/h) and magnitude[6-7]. Figures (a) and (b) present the results of a walking human and a moving vehicle. In case of moving vehicle, we can see the sharp Doppler spectra. But, in case of walking human, the shapes of them are very wide and variable. Based on such characteristics, we designed the target classification algorithm and verified the scheme. In case using only feature vector

extracted from spectrum width, we can obtain classification rate as 81% about single target. If we employed three feature vectors studied in the previous work [8], we expect the classification performance can be increased.

4. Conclusions

In this paper, we developed a HW and SW platform to verify the radar front-end module and signal processing algorithm. The developed system was tested with a 24-GHz multiple-channel FMCW FEM based on stationary and moving target scenarios in a test chamber. First, we checked the real-time data-logging operation. In the measurement results, we also could see that radar data normally were logged and the range-profiles were exactly extracted using a basic signal processing algorithm. Moreover, we verified human classification algorithm using the real measurement data.

In the future, based on the developed hardware and software platform for read verification, we will implement and test various radar algorithms. We expect that this can be very advantageous because real-time test and monitoring is possible.

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